REMARKS

Claim Rejections Under 35 U.S.C. § 102

Claims 1-44 were rejected under 35 U.S.C. § 102(e) as being clearly anticipated by Nobunaga et al. (U.S. Patent No. 6,304,510). Applicant strongly traverses this rejection. This exact reference has been used in a previous office action, mailed October 27, 2004. At that time, Applicant clearly showed how the reference did not contain each and every element of the claims. In a second office action mailed March 21, 2005, in response to the first office action response, claims 1-8, 12-34, and 38-44 were allowed, and claims 10-11 and 36-37 were objected to but were indicated to contain allowable subject matter. The office action stated that the claims were not taught by the cited art. Now, with no further amendment, the new office action presents the nearly identical rejection as was used in the first office action, which was overcome by the first response by Applicant, and was acknowledged to be overcome in the second office action.

Applicant repeats its arguments that Nobunaga et al. does not teach each and every element of the claims. Specifically, the claims recite configuring the addressable banks in response to a program state of the mode register. The current office action asserts that column 4, lines 26-43 of Nobunaga et al. discuss configuration of addressable banks. Applicant has read and re-read the reference, and column 4, lines 26-43, and fails to find any mention whatsoever of configuring addressable banks. Column 4, lines 26-43 are directed to the use of mode register 148 (which does not appear in any of the Figures of Nobunaga et al., but which is presumed to be part of command execution logic 130) to define the specific mode of operation of the memory, including the selection of a burst length, a burst type, CAS latency, and an operating mode. Nowhere is configuration of the addressable banks, as required by the claim, shown or described. The banks of the present claims are configurable based on a program state of the mode register in claim 1. The configuration allows the configuration of the number of banks in the memory. Nowhere in Nobunaga et al. is there even the slightest discussion or teaching of the configuration of the number of banks of a memory. Each and every embodiment and figure that shows anything at all about the banks of Nobunaga et al. shows and discusses four banks. There is no possible reading of Nobunaga et al. that allows for the configuring the addressable banks as is recited by the claims.

Nobunaga et al. is directed generally to memory device address decoding. In contrast, the present application is directed generally to configuration of the number of banks in a memory, and the associated structure and methods to accomplish that.

With reference to the entire pending claim set and the rejections thereof, Applicant submits that nowhere in Nobunaga et al. is any mention made at all of configuring the number of banks in a memory. In fact, nowhere in Nobunaga et al. is there made any mention of any memory that does not have four banks. The Office Action itself asserts that Figure 1 shows either four or eight banks. In fact, Figure 1 and the accompanying text of the Nobunaga et al. specification clearly and unambiguously show and describe four banks, namely banks 104, 106, 108, and 110. There is no mention of reconfiguring the number of banks, and there is certainly no mention of the same physical structure being configurable into a different arrangement of banks, as is the subject generally of the pending claims. Further, the assertion that status register 130 is a "mode register" that performs the functions of the mode register identified and recited in the present claims is wholly unsupported by the specification and figures of Nobunaga et al.

The "mode register" 130 of Nobunaga et al. is identified as a command execution logic including a status register 134 and an identification register 136, neither of which operate to "configure the addressable banks" as is recited in claim 1, to "configure the array in response to a program state of the mode register, wherein the mode register defines a number of addressable banks of the array" as is recited in claim 4, or routing a selected address to either the row or bank address decoder "in response to data stored in the mode register" as in claim 9. Further, Nobunaga et al. contains no teaching or disclosure of configuring the addressable banks in any way. Claims 1, 4, and 9 are allowable. Claims 2-3, 5-8, and 10-11 depend from and further define one of patentably distinct claims 1, 4, or 9, and are also believed allowable.

Still further, there is no mention of changing the number of bank in the memory in Nobunaga et al. as is required by claim 4. The assertion of the office action that column 3, lines 64-67, column 4, lines 1-5 and Table 1 have anything at all to do with changing the number of banks of the memory of Nobunaga et al. is wholly unsupported . There is no mention at all of changing the number of banks of the memory anywhere in Nobunaga et al., much less in column 3, lines 64-67, column 4, lines 1-5 and Table 1.Those sections discuss population densities of a memory, read accesses, and definitions of bursts, not the changing of the number of banks in the memory. Claim 4 is allowable.

Claim 12 recites "logic circuitry" that works with the address signal circuitry to route a selected address input connection to the row or bank address decoder in "in response to the logic

circuitry." This is not present anywhere in Nobunaga et al. As such, claim 12 is allowable. Claims 13-15 depend from and further define patentably distinct claim 12, and are also believed allowable.

Claim 16 recites "a decode circuit" and address circuitry that configures the addressable banks "in response to a program state of the input signal." Once again, Nobunaga et al. contains no mention or teaching whatsoever of configurable banks or a system containing the elements of the claim. Claim 16 is allowable. Claims 17-21 depend from and further define patentably distinct claims 16, and are also believed allowable.

Claims 22 and 30 each recite that the "input signal defines a number of addressable banks of the array." Claim 27 recites address circuitry "to configure the addressable banks in response to a program state of the external input signal." Claims 38 and 42 each recite that "the address circuitry configures a number of addressable banks of a memory cell array." As has been repeatedly shown above, Nobunaga et al. contains no such teaching or disclosure. As such, claims 22, 27, 30, 38, and 42 are allowable. Claims 23-26, 28-29, 31-34, 39-41, and 43-44 depend from and further define one of patentably distinct claims 22, 27, 30, 38, or 42, and are also believed allowable.

Claim 35 recites that "the address signal circuitry routes a selected on of the plurality of address input connections to either the row or bank address decoder in response to data decoded by the decode circuit." Once again, there is no such teaching in Nobunaga et al. Claim 35 is allowable. Claims 36-37 depend from and further define patentably distinct claim 35, and are also believed allowable.

CONCLUSION

Applicant respectfully submits that the claims remain allowable. They were nearly all allowed over Nobunaga et al. after Applicant's response to the first office action. Nothing has changed. The Nobunaga et al. reference did not then contain a disclosure that teaches each and every element of the claims, and it does not now contain any disclosure that teaches each and every element of the claims. The claims are allowable. If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2203.

Respectfully submitted,

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